that various nodes in the buffer may maintain a voltage level corresponding to a normal state, during the charge sharing section.

[0141] FIG. **17** is a block diagram of a touch display driving circuit **1100** according to an exemplary embodiment.

[0142] As illustrated in FIG. **17**, the touch display driving circuit **1100** may be realized as one semiconductor chip, and thus, a display driving function for driving the panel and a touch control function for controlling a touch operation may be integrated into one semiconductor chip. For example, the touch display driving circuit **1100** may include a touch controlling unit **1110** (e.g., touch controller) and a display driving unit **1120** (e.g., display driver).

[0143] Since the touch controlling unit **1110** and the display driving unit **1120** are integrated into one semiconductor chip, the touch controlling unit **1110** and the display driving unit **1120** may exchange various types of information or signals via wirings in the semiconductor chip. For example, the touch controlling unit **1110** and the display driving unit **1120** each may provide state information indicating a state thereof. Also, the display driving unit **1120** may provide information indicating various timings related to the display driving, and the touch controlling unit **1110** may provide information indicating various timings related to the touch operation. Also, when a function block for generating power is included in the display driving unit **1120**, the display driving unit **1120** may provide power to the touch controlling unit **1110**. According to an exemplary embodiment, the provision of power of the display driving unit **1120** may be controlled based on various types of information exchanged between the display driving unit **1120** and the touch controlling unit **1110**.

[0144] The touch controlling unit **1110** may include various function blocks which are respectively configured to perform predetermined functions. For example, the touch controlling unit **1110** may include an analog front end (AFE) that reads a signal of a sensing unit (e.g., sensor), a memory, a main control unit (MCU) (e.g., main controller), a control logic, etc. Also, the display driving unit **1120** may include a control logic, a display memory, a power generating unit, a source driver, etc. The source driver may include the buffer unit **1121** according to the exemplary embodiment. Buffers included in a buffer unit **1121** may include a feedback path (for example, a negative feedback path), and a connection switch is additionally disposed between various nodes in the buffer (for example, an amplification unit). During a charge sharing operation, the connection switch is turned on, and thus, voltage levels of various nodes in the buffer are adjusted so that various nodes in the buffer may maintain a voltage level corresponding to a normal state during the charge sharing operation.

[0145] While the exemplary embodiments have been particularly shown and described with reference to certain exemplary embodiments thereof, it will be understood that various changes in form and details may be made therein without departing from the spirit and scope of the following claims.

1. A source driver comprising:

a buffer device comprising a plurality of buffers corresponding to a plurality of data lines, wherein each of the plurality of buffers respectively comprises an amplifier configured to amplify an input signal and an output driver configured to output a driving signal to a corresponding data line among the plurality of data lines; and

a switch device comprising a charge sharing switch configured to electrically connect the plurality of data lines to one another during a charge sharing operation,

wherein each of the amplifiers comprises a first current mirror having a reference current path comprising a first node and an output current path comprising a second node, and

the first node of the reference current path and the second node of the output current path are electrically connected to each other during the charge sharing operation.

2. The source driver of claim **1**, wherein the amplifier further comprises a first switch connected between the first node and the second node, and

the first switch is turned on during the charge sharing operation.

3. The source driver of claim **2**, further comprising a control logic configured to generate a first control signal for disabling the output driver and a second control signal configured to turn on the first switch during the charge sharing operation.

4. The source driver of claim **1**, wherein the output driver is disabled during the charge sharing operation.

5. The source driver of claim **1**, wherein the plurality of buffers are provided in a path which negatively feeds back the driving signal from an output end to an input end of the plurality of buffers.

6. The source driver of claim **5**, wherein voltage levels of the first node and voltage levels of the second node during the charge sharing operation correspond to voltage levels of the plurality of buffers during a normal state.

7. The source driver of claim **1**, wherein the amplifier further comprises a second current mirror having a reference current path comprising a third node and an output current path comprising a fourth node, and

in the second current mirror, the third node of the reference current path and the fourth node of the output current path are electrically connected to each other during the charge sharing operation.

8. The source driver of claim **1**, wherein the amplifier further comprises a bias device,

the reference current path comprises a first transistor comprising a first gate and a second transistor comprising a second gate, the first transistor and the second transistor being connected in series to each other between a first voltage and the bias device,

the output current path comprises a third transistor comprising a third gate and a fourth transistor comprising a fourth gate, the third transistor and the fourth transistor being connected in series to each other between the first voltage and the bias device, and

the first gate of the first transistor is connected to the third gate of the third transistor, and the second gate of the second transistor is connected to the fourth gate of the fourth transistor.

9. The source driver of claim **8**, wherein the first node is provided between the first transistor and the second transistor, and the second node is provided between the third transistor and the fourth transistor.